IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: David Qiang Meng	Art Unit	: 2187
Serial No.	: 10/750,423	Examiner	: Jared Ian Rutz
Filed	: December 30, 2003	Conf. No.	: 4620
Title	: PARTITIONING MEMORY		

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REPLY BRIEF

Pursuant to 37 C.F.R. § 41.41, Applicant responds to the Examiner's Answer as follows.

Appellant acknowledges that the examiner has withdrawn the rejection of claims 1-26 under 35 U.S.C 101.

Claim 1

In answer to Appellant's argument with respect to claim 1, the examiner states:

> **The Examiner respectfully notes that claim 1 requires partitioning a memory device to produce a first group of memory entries and a second group of memory entries. The entries of the first group are required to be accessible in parallel, and selectable independent of the second group of memory entries. The entries of the second group are also accessible in parallel.**
>
> **The Examiner respectfully points out that the section of the specification cited by Applicant contains no discussion of partitioning a memory device to produce the two groups of memory entries required by claim 1. The cited section of the specification discusses partitioning a single memory entry into two or more subentries. It would appear that Applicant would have the board believe that the subentries discussed in the cited portion of the specification correspond to the entries recited in claim 1. However, the Examiner respectfully points out that claim 2 further recites that a memory entry is partitioned into sub-entries. The cited portion of the specification discusses grouping subentries which can be selected independently and accessed in parallel, but there is no mention of memory entries being partitioned as claimed, let alone a description which would enable one of ordinary skill in the art to make the claimed invention.[1]**

[1] Examiner's Answer pages 12-13

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The examiner's contention that "**the section of the specification cited by Applicant contains no discussion of partitioning a memory device to produce the two groups of memory entries required by claim 1. The cited section of the specification discusses partitioning a single memory entry into two or more subentries.**"[2] is not the support relied on for enablement. Appellant was confused by the examiner's terse arguments in that the examiner did not specifically point out what groups the examiner had alluded to.

In the Appeal Brief, Appellant in response argued the features of partitioning of the entries and also argued features of the partition of the memory into entries.[3] The examiner having clarified the rejection, in answer to Appellant's Brief, allows the Appellant to understand that it was the partition into entries and not subentries that was the examiner's concern.

Support for the feature of the partition of entries is depicted in each of FIGS. 4, 7-9. In Appellant's specification, the support for these partitions is described, for example, as follows.

> CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period (e.g., clock cycle) to determine if particular data is present in one of the entries. For example, to route a received packet (e.g., packet_1) to its intended destination, a destination address stored in the packet is compared in parallel to addresses stored in the CAM 54 entries. If a match is detected, the particular CAM entry storing the matching data is used to identify a corresponding location in local memory 56. For example, if an address (e.g., a media access control (MAC) address) associated with a received packet matches data (e.g., MAC address 0) stored in CAM entry 0, the CAM entry identifies a location in the local memory 56 that stores data (e.g., an Internet Protocol (IP) address) for directing the packet to its intended destination. If a match is not found, appropriate data (e.g., IP address) for directing the packet are retrieved from memory external to the packet engine (e.g., DRAM) and stored in the local memory 56. Also to direct other packets intended for the same destination, the unmatched address (e.g., MAC address) is stored in one of the CAM 54 entries. In some arrangements, the contents of the "Least Recently Used" (LRU) CAM entry is replaced with the unmatched address, however,

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[2] Id.
[3] Appeal Brief page 10.

> other arrangements may implement other CAM entry selection techniques.[4]

Appellant previously pointed out this support.[5] These partitions are a matter of association by the CAM manager of, e.g., IP address ranges to specific entries **(e.g., MAC address 0) stored in CAM entry 0, the CAM entry identifies a location in the local memory 56 that stores data (e.g., an Internet Protocol (IP) address).**[6]

The features of Claim 1 are supported, as outlined in bold herein. Claim 1 recites the feature of: "partitioning a memory device **"content-addressable memory (CAM) 54"**[7] to produce a first group of memory entries "**in CAM 60 is shown Entry 0.**"[8] being accessible in parallel and selectable independent of "**In this example, each of the thirty-two CAM 54 entries includes a 32-bit portion for storing data (e.g., MAC addresses) for comparing in parallel with other data (e.g., a MAC address associated with a received packet).**"[9] a second group of memory entries in the memory device that is accessible in parallel. "**(CAM 60 is shown with Entry 2."**[10]

The examiner overlooks the functionality of a content addressable memory[11] and the convention of partitioning of memory. However, Appellant provides a novel partition of a memory that is useful, for example, in processing of network packets.[12]

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[4] Appellant's specification page 8, line 7.
[5] See note 1.
[6] Id. line 19.
[7] Appellant's specification page 8, line 4.
[8] FIG. 4. See also Appellant's specification, page 9, lines 18-22
[9] Id. page 9, line 8.
[10] FIG. 4. See also Appellant's specification, page 9, lines 18-22
[11] See http://en.wikipedia.org/wiki/Content-addressable_memory in the enclosed Information Disclosure Statement.

> Unlike standard computer memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found (and in some architectures, it also returns the data word, or other associated pieces of data). Thus, a CAM is the hardware embodiment of what in software terms would be called an associative array.

[12] Appellant's specification page 8, line 11.

Therefore, while the examiner correctly noted that: "**The ... section of the specification cited by Applicant contains no discussion of partitioning a memory device to produce the two groups of memory entries required by claim 1.**"[13], the examiner erroneous overlooked the section referred to above. Therefore, despite the confusion of what the examiner argued was not enabled, the feature of claim 1 is nonetheless enabled and described within the meaning of 35 U.S.C. 112, first paragraph.

Claim 8 being the computer program product analogue of claim 1 and claim 15, being the memory manager analogue of claim 1 are supported as in claim 1. Claim 18 being a system possessing a memory that is the analogue of claim 1 and claims 21, a packet forwarding device and claim 24 a content addressable memory each being respective analogues of claim 1 are likewise supported, as set forth above for claim 1.

Claim 2

The examiner also argues that:

> **However, the Examiner respectfully points out that claim 2 further recites that a memory entry is partitioned into sub-entries. The cited portion of the specification discusses grouping subentries which can be selected independently and accessed in parallel, but there is no mention of memory entries being partitioned as claimed, let alone a description which would enable one of ordinary skill in the art to make the claimed invention.** [14]

Given the clarification above, Appellant points out that the specification discusses "partitioning individual entries into two or more subentries,"[15] and therefore the examiner now must take all of the subject matter as being enabled. Clearly, the specification discusses partitioning of individual entries into two or more subentries and clearly shows those in the figures.

Appellant's specification disclosure that: "The CAM manager 58 is capable of partitioning individual entries into two or more subentries that are individually selectable for use in parallel comparisons. By producing subentries, particular ones of the subentries are grouped

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For example, to route a received packet (e.g., packet_1) to its intended destination, a destination address stored in the packet is compared in parallel to addresses stored in the CAM 54 entries.

[13] Examiner's Answer page 13

[14] Id.

[15] Id.

for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel."[16], describes and enables this feature of claim 2.

Appellant did not seek to: "**,,,, have the board believe that the subentries discussed in the cited portion of the specification correspond to the entries recited in claim 1.**"[17] Appellant has clarified its argument based on the clarification of the rejection raised by the examiner. Therefore, claim 1 is enabled and described by Appellant's specification because in fact Appellant describes and enables partitioning of entries, as discussed above, and has described and enabled partitioning of the subentries as in claim 2.

The examiner also argues that:

> **Again, the cited section of the specification does not discuss how to partition the 32 entries of CAM 54 into a first and second group as recited in the claims. There is a statement that the CAM manager partitions the CAM into a particular number of entries. However, there is no explanation of what steps are necessary to perform the recited partitioning, and there is no explanation of what causes one group of entries to be selectable independently of another group of entries.**[18]

Appellant contends that in view of the discussion in the Appeal Brief that how to partition the 32 entries is quite evident as an association of IP addresses to entries, as discussed above.

Appellant also argued that the examples of how the CAM is partitioned and used are set out throughout Appellant's specification in that various partitions of entries and sub-entries are depicted in Appellant's FIGS. 4-7. In response the examiner argues:

> **The Examiner respectfully notes that figures 3-7 show a plurality of examples of a CAM, which is shown as a rectangle. Each CAM is shown containing a number of rectangles. In figures 3 and 7, each rectangle within the CAM is identified as an entry. In figures 4 and 6, entries are formed of two rectangles. In figure 5, three or more rectangles appear to be grouped into entries. Figures 3-7 show no hardware which would support making one group of entries selectable in parallel independently of another group of entries, and, in fact, do not appear to show**

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[16] Appellant's specification page 9, line 23.
[17] Examiner's Answer page 13.
[18] Id. page 14.

> **entries partitioned into groups. Further, it is unclear from the description and the drawings what each rectangle within the CAM is, per se.**[19]

Appellant contends that it is conventional and acceptable for an application in this field of endeavor to use block diagrams and flow charts to describe the salient features of computer software and hardware. However, the examiner errs in arguing that Appellant does not show hardware that would support the claimed features.[20] Clearly, Appellant shows a CAM 54 and a CAM manager 58 and describes that: "… CAM manager 58 is implemented as microcode in the control store 50 and, which is executed by the packet engine 48. The CAM manager 58 partitions the CAM 54 into a particular number of entries."

Nevertheless, the Examiner mistakenly assumes that some huge "modification to a known prior art CAM would be necessary to implement the claimed invention." Rather, the modification needed to distinguish the Handy CAM from claim 1 is to configure the CAM with the partitions by the CAM manager, as pointed out above.

The ability to be partitioned into two groups of entries as recited in the claims results from a combination of the CAM manager and the functional aspects of a CAM. There are not modifications required to the CAM, but rather configuration by the CAM manager of the CAM and partition of the entries according to, e.g., IP and MAC addresses as mentioned above and as clearly discussed in the specification, as argued above.

The examiner misconstrues page 11 line 19 through page 12 line 1 stating: **"By allowing CAM 54 to load different data types (e.g., MAC addresses, IP addresses) into each CAM entry and to select which data type to use to determine a potential match, the CAM can be loaded during one time period with two or more different data types compared to loading the CAM multiple times with different data types for separate parallel comparisons in an unconfigurable CAM."**[21] Rather, it is the loading of different data types that provides the independence the examiner does not appreciate, thus permitting IP Address to be selected independently of MAC addresses, for instance.

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[19] Id. page 15.
[20] The examiner relies on *In re Ghiron*, 442 F.2d 985, 991-92, 169 USPQ 723, 727-28 (CCPA 1971), for the proposition that functional "block diagrams" were insufficient to enable a person skilled in the art to practice the claimed invention. Appellant doubts that the guidance in this case is still useful.
[21] Examiner's Answer page 16.

The Examiner acknowledges that memory partitioning, per se, is known to one of ordinary skill in the art. The examiner also argues that:

> **There is no prior art of record that would indicate that this particular configuration of memory partitioning is known. Applicant, by virtue of reciting this particular configuration as the sole step of the method recited in step 1, is alleging that this particular configuration of memory configuration is not known to one of ordinary skill in the art. If this particular configuration of memory configuration is known in the art, as argued by Applicant in the cited section of the Appeal Brief, then it would appear that Applicant has failed to claim what Applicant considers their invention.**[22]

This however, in Appellant's view is the examiner's real issue. The prior art, as far as the examiner can tell, neither describes nor suggests the feature of claim 1. Nonetheless, in Appellant's opinion, the examiner feels compelled to force Appellant to limit the scope of the claims by requiring amendments based on an alleged lack of enablement. Appellant contends that this is wholly improper. Appellant has not claimed these features in means plus function language, in an attempt to usurp all possible means for performing the cited feature. Rather, Appellant has recited a single, positive step, which is permitted, even by the Board's own precedents.[23]

The examiner argues that Appellant's prior argument "**…seems to imply that the claimed partitioning is well known in the art; further suggesting that the instant application does not claim what Applicant considers their invention.**"[24] This was not the thrust of Appellant's argument. Rather, the argument was that partitioning *per se* was well-known. If the particular partition of claim 1 was well-known, Appellant would not have only recited that feature in claim 1.

The examiner also argues that: **The Examiner acknowledges that, as discussed in M.P.E.P. 2164.01(a), *In re Wands* sets forth 8 factors that must be considered. Although not expressly set out in the Final Office Action, the Examiner respectfully notes that several of the factors were addressed.**[25] The examiner had not addressed most, if any, of factors in the rejections and thus had not afforded Appellant reasonable notice and opportunity to adequately respond.

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[22] Id. page 18
[23] The claims need not provide all operating details but a method claim should recite a positive step. *In re Erlich*, 3 U.S.P.Q. 2d 1011 (Bd. Pat. App. & Int., 1986).
[24] See note 22.
[25] Examiner's Answer page 19.

Nevertheless, Appellant responds to these 8 *Wands* factors as set out by the examiner, as follows:

The breadth of the claims

The Examiner argues that the only disclosed embodiment is a CAM which is partitioned by microcode, and that Appellant does not teach "**one of ordinary skill in the art how to make the claimed invention using a RAM or a ROM, which are not known to have entries which are accessible in parallel.**"[26] Appellant does not understand the point of this argument, but to possible attempt to limit the subject matter to "content addressable memories," rather than "memories," as in claim 1. As an initial observation, Appellant points out that the standard is not of "ordinary skill," but "one skilled in the art." Appellant also points out that a CAM is a memory device and that it is a specialized memory that is implemented by RAM.[27] Therefore, Appellant contends that claim 1, which calls for a memory,[28] is not overly broad and indeed is supported by Appellant's disclosure. Clearly, one of the benefits to Appellant claiming of a memory is to avoid "wordsmanship" gaming of the subject matter by infringers that would argue had claim 1, been limited to a CAM, that the accused infringing device did not include a CAM.

The nature of the invention

The Examiner argues that " **...the nature of the invention, as recited in independent claims 1,8, 15, 18, 21, and 24, is a configurable CAM, as discussed in the specification at page 11 line 19 through page 12 line 1.**"[29]

Appellant contends that the nature of the invention of claim 1 is that of specific partition of a memory device.

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[26] Id.
[27] See Article cited in accompanying IDS.
[28] Not all of Appellant's claims and indeed independent claims are limited to a "memory." For instance, independent claims 15 and 24 are directed to content addressable memories, but have received no differing treatment from the examiner.
[29] Examiner's Answer page 20

The state of the prior art

The Examiner argues that: "**The Examiner respectfully submits that the Handy reference has been submitted to illustrate what was known by one of ordinary skill in the art as a CAM. The Examiner further notes that Applicant has submitted no evidence to indicate that a configurable CAM as claimed was known to one of ordinary skill in the art.**"[30]

Claim 1 does not specify a "configurable CAM," as the examiner appears to use that phrase, as being somehow different that a conventional CAM. Appellant's specification, where the examiner appears to be confused makes a comparison of the arrangement of the CAM into the claimed partitions with the different data types.[31] Again, the examiner appears to misconstrue Appellant's teachings.

The level of one of ordinary skill

The examiner states: "**The Examiner respectfully submits that there is only one distinct technology relevant to the claimed invention, electronic computer memory systems.**"[32] Appellant does not believe that this statement is at all relevant or probative of the level of one of ordinary skill in the art. Appellant contends that the standard is skilled in the art and that the level of that skill is very high.

The level of predictability in the art

Appellant agrees with the examiner "**that the electronic computer memory art is fairly predictable.**"[33]

The amount of direction provided by the inventor

The Examiner argues that: "**...the only direction provided by the inventor is that the CAM manager partitions the memory, and that the CAM manager may be implemented as microcode that may be executed on the packet processor at page 9 lines 18-22 of the specification. ...** "[34] Appellant has address this above.

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[30] Id.
[31] Appellant's specification page 12, line 19
By allowing CAM 54 to load different data types (e.g., MAC addresses, IP addresses) into each CAM entry and to select which data type to use to determine a potential match, the CAM can be loaded during one time period with two or more different data types compared to loading the CAM multiple times with different data types for separate parallel comparisons in an un-configurable CAM.
[32] Examiner's Answer page 20
[33] Examiner's Answer page 20
[34] Id.

The Examiner also argues that "... **the inventor has not provided any indication of what steps would need to be performed by the CAM manager to partition the CAM as claimed, what, if any, hardware modifications would need to be made to an un-configurable CAM to make it - into a configurable CAM, and what, if any signals would the CAM manager need to provide to a configurable CAM to configure the CAM.**" Appellant has address this above with respect to hardware modifications and configurable. With respect to signals and steps, Appellant does not see where signals would fit into this description and with respect to steps they are shown in Appellant's Figures and described in the accompanying description. In addition, the various partitions are illustrated and enabled in the Figures and the accompanying description, as discussed above.

The existence of working examples

The Examiner argues that: "**The Examiner is not aware of any working examples of the claimed invention, and respectfully submits that the specification does not contain detail of a configurable CAM to the level that would indicate the existence of a working example.**"[35] Appellant notes that these are not needed in general and in particular in predictable arts. Nonetheless examples are shown in the figures 4-7.

The quantity of experimentation needed to make or use the invention based on the content of the disclosure

Appellant contends that the examiner's argument that "**the quantity of experimentation needed by one of ordinary skill in the art having the disclosure of the instant application to make the claimed invention would be approximately equivalent to the quantity of experimentation required by the inventor to initially invent the claimed invention.**"[36] is totally without merit. The specification provides clear guidance on the functioning of the microcode embodying the CAM manager, as discussed above. The examiner argues that Appellant fails to show how "**to modify the hardware of a known prior art CAM to make a CAM that may be configured by the CAM manager,**"[37] is without merit and based on a complete misconception of the subject matter of the specification and the claims, as pointed out above.

The examiner also argues that:

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[35] Id. page 21
[36] Id.
[37] Id.

> **The Examiner respectfully submits that Applicant provides no further arguments as to how "partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel" as recited in claim 1 is enabled by the disclosure of the instant application.[38]**

However, the examiner ignores that since a CAM searches all entries, it automatically searches in parallel, at least at the level of the subject matter of the claims.

35 U.S.C. 112 first paragraph, written description requirement

The Examiner argues that:

> **...To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. See, e.g., Moba, B.V. v. Diamond Automation, Inc., 325 F.3d 1306,1319, 66 USPQ2d 1429, 1438 (Fed. Cir. 2003); Vas-Cath, Inc. v. Mahurkar, 935 F.2d at 1563, 19 USPQ2d at 1116. Possession may be shown in a variety of ways including description of an actual reduction to practice, or by showing that the invention was "ready for patenting" such as by the disclosure of drawings or structural chemical formulas that show that the invention was complete, or by describing distinguishing identifying characteristics sufficient to show that the applicant was in possession of the claimed invention. See, e.g., Pfaff v. Wells Elecs., Inc., 525 U.S. 55, 68, 119 S.Ct. 304, 312, 48 USPQ2d 1641, 1647 (1998).[39]**

Appellant respectfully submits that the examiner has not presented any applicable authority that requires proof of an actual reduction to practice of the subject matter of claims in predictable arts, because the examiner has incorrectly applied reasoning of the so called Lilly rule.[40] There is no requirement that in predictable arts of an actual reduction to practice of the invention to satisfy the written description requirement, and to show that the inventor had possession of the claimed invention. The specification contains numerous descriptions of how a memory such as a CAM stores MAC addresses and IP addresses for access independently and in parallel, and specification shows how the actual claimed partitioning is performed, as set out above.

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[38] Id. page 22
[39] Id. page 23
[40] In Regents of the University of California v. Eli Lilly & Co. (119 F.3d 1559, 43 USPQ2d (BNA) 1398 (Fed. Cir. 1997), cert. denied, 523 U.S. 1089 (1998)), the court found that a patent did not provide adequate WD for claims directed to the sequence of genes that encodes human insulin.

For these reasons, and the reasons stated in the Appeal Brief, Applicant submits that the final rejection should be reversed.

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Respectfully submitted,

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